Accordingly, the amendments do not introduce new matter, and entry is respectfully requested.

In addition, Applicant has addressed the rejection under 35 U.S.C. §112, second paragraph, by deleting the objected-to language.

Applicant wishes to express their appreciation to SPE Utech, for taking the time to discuss this case with undersigned counsel on January 29, 2002, in Examiner Perez-Ramos' absence. The amendments set forth above were discussed during the interview, and it was agreed that this would overcome the prior art rejection, as well as meet the rejection under 35 U.S.C. §112, second paragraph.

In particular, the art over which the claims stand rejected, U.S. Patent 5,853,602, Shoji, teaches directly away from the claimed invention, in specifying a second stage etching, which employs a gaseous etchant comprising fluorine as a principle etching agent. See in particular, column 5, lines 6-11:

> Subsequently, the semiconductor structure shown in Figure 5B is subjected to a second-stage etching, and gaseous etchant of SF_6, Cl_2, and O_2 is used in the second-stage etching.

This disclosure is consistent with the object of Shoji, which is to achieve tungsten removal, in which process fluorine is essential.

Accordingly, as the claims are directed to a process that excludes fluorine from the second stage etch, and the prior art requires fluorine for a corresponding etch, the claims are believed patentably defined over the reference.

All other rejections and objections having been met, it is believed that the claims are directed to allowable subject matter, and otherwise in conformance with the requirements of Tile 35. Accordingly, a favorable action thereon is respectfully solicited.

Respectfully submitted,

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MARKED-UP COPY OF AMENDED CLAIMS

1. A method for etching a semiconductor device to form [a predetermined] an etched pattern therein, comprising:

(a) providing a semiconductor device having a plurality of layers, at least one of the layers of the semiconductor device comprising a refractory metal-containing material; and

(b) etching the semiconductor device under conditions with an etchant composition comprising a first etchant chemistry which comprises a chlorine source and a second etchant chemistry which is free of fluorine, [providing a uniformity across the plurality of layers of ± about 3.5 percent].

15. A method of etching a refractory metal-containing layer and an oxide layer, the method comprising:

(a) etching the refractory metal-containing layer to an end point using a first etchant chemistry at a source power of from about 100 watts to about 450 watts and a bias power of from about 200 watts to about 500 watts, wherein the first etchant chemistry comprises a chlorine source and a fluorine source; and

(b) etching partially through the oxide layer using a second etchant chemistry, wherein the second etchant chemistry is free of fluorine and comprises a chlorine source.

31. A method of etching a semiconductor device using a capacitive coupling plasma reactor to form a [predetermined] pattern on the semiconductor device, comprising:

(a) providing a semiconductor device having a plurality of layers, at least one of the layers

of the semiconductor device comprising a refractory metal-containing material; and

(b) etching the semiconductor device with an etchant composition at a bias power of from about 100 watts to about 750 watts, wherein the etchant composition comprises a first etchant chemistry comprising chlorine and a second etchant chemistry free of fluorine.